The present invention is related to subject matter disclosed in the following co-pending patent applications:

1. United States patent application serial no. 09/204,480 entitled, "A Multiple-Thread Processor for Threaded Software Applications", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998;

2. United States patent application serial no. 09/204,584 entitled, "Clustered Architecture in a VLIW Processor", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998;

3. United States patent application serial no. 09/204,481 entitled, "Apparatus and Method for Optimizing Die Utilization and Speed Performance by Register File Splitting", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998;

4. United States patent application serial no. 09/204,536 entitled, "Variable Issue-Width VLIW Processor", naming Marc Tremblay as inventor and filed on December 3, 1998;

5. United States patent application serial no. 09/205,121 entitled, "Dual In-line Buffers for an Instruction Fetch Unit", naming Marc Tremblay and Graham Murphy as inventors and filed on December 3, 1998;

6. United States patent application serial no. 09/204,781 entitled, "An Instruction Fetch Unit Aligner", naming Marc Tremblay and Graham Murphy as inventors and filed on December 3, 1998;

7. United States patent application serial no. 09/204,535 entitled, "Local Stall Control Method and Structure in a Microprocessor," naming Marc Tremblay and Sharada Yeluri as inventors and filed on December 3, 1998;

8. United States patent application serial no. 09/204,585 entitled, "Local and Global Register Partitioning in a VLIW Processor", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998; and